IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: Michael Trinh	
Serial No.:	09/256,643	Group Art Unit: 2822	
Filed:	February 23, 1999	Docket: 303.324US2	
Title:	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE		

RESPONSE UNDER 37 CFR § 1.111

32nd Response 11/25/02 L Brown

Commissioner for Patents
Washington, D.C. 20231

In response to the Office Action dated 13 August 2002, the applicant respectfully requests reconsideration of the above-identified application in view of the following remarks. Claims 21, 23, 24, 26, 29-33 and 36-75 are pending in the application. Claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 are rejected, and claims 33, 47, 62, 67, 70, and 75 are objected to. None of the claims have been amended.

Telephone interview

The applicant thanks Examiner Trinh for the telephone interview granted on Tuesday, 12 November 2002 between himself and the applicant's representative Mr. Mates (Reg. No. 35,271). The substance of this response was discussed during the interview.

Allowable Subject Matter

The Office Action indicated that claims 33, 47, 62, 67, 70, and 75 would be allowable if rewritten in independent form. The applicant reserves the right to rewrite claims 33, 47, 62, 67, 70, and 75 in independent form, but believes that the base claims from which they depend are allowable in view of the remarks made herein.

Rejections Under 35 USC § 103

Claims 21, 23-26, 29-32, 36-46, and 48-59 were rejected under 35 USC § 103(a) as being unpatentable over Chamberlain (U.S. Patent No. 4,473,836) taken with Halvis et al. (U.S. Patent No. 5,369,040, Halvis). The applicant respectfully traverses.

Chamberlain shows a photodetector structure shown in Figure 2 including a silicon substrate 11 having a diffused photosensitive region D1 that functions as a source and a diffused

region D2 that functions as a drain. Chamberlain, column 3, lines 10-15.

Halvis shows a MOS photodetector with gates 34, 36, 38, 48, and 50 shown in Figure 4C. The gates comprise polysilicon and carbon.

"To establish a *prima facie* case of obviousness ... there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." The suggestion or motivation to combine references must be found in the prior art. MPEP 2143.

Chamberlain states the following:

> "In the embodiment illustrated gate G1 includes a layer 13 of SiO_2 overlaid by a layer of aluminum or polysilicon 14. If polysilicon is employed, it must be covered to be impervious to light, since polysilicon is transparent." Chamberlain, column 3, lines 23-26.

Chamberlain also states:

> "It is important to note that all parts of the photodetector structure are shielded from light except for region D1, the upper surface of which receives and is exposed to light." Chamberlain, column 3, lines 39-44.

According to Chamberlain the gate G1 must shield the photodector from light, and may be covered to do so.

The polysilicon and carbon gate of Halvis with which the Office Action proposes to replace the gate G1 of Chamberlain is transparent to visible light:

> "this invention describes a MOS photodetector which has gates fabricated from polysilicon with the addition of carbon .... which makes the gate material more transparent to the visible portion of the energy spectrum..." Halvis, column 2, lines 18-24.

Halvis also says:

> "By adding carbon to the polysilicon material of a MOS photodector device, the amount of visible light absorbed by the gate material can be reduced, and the quantum efficiency of the detector can thereby be improved." Halvis, column 3, lines 30-35.

Halvis describes a gate that absorbs less visible light and is therefore more transparent to visible light.

The Office Action stated that the motivation for this combination was language in Halvis relating to the need for photodetectors with "improved quantum efficiency" and "improved response" and "improved performance" and "improved sensitivity." Halvis, column 1, line 64 to column 2, line 17. However, the "improved quantum efficiency" shown by Halvis is due to the gate of Halvis being more transparent to light. Chamberlain expressly states that his gate must shield the photodector from light, and therefore must block light. One skilled in the art would **not** be motivated to add carbon to the gate of Chamberlain to make it more transparent to visible light because the gate of Chamberlain must block the light or be covered so as to block the light.

There is no suggestion for this combination of references.

The applicant respectfully submits that a *prima facie* case of obviousness of claims 21, 23-26, 29-32, 36-46, and 48-59 has **not** been established in the Office Action, and that claims 21, 23-26, 29-32, 36-46, and 48-59 are in condition for allowance.

Claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 were rejected under 35 USC § 103(a) as being unpatentable over Yamazaki et al. (U.S. Patent No. 5,449,941, Yamazaki) in view of Halvis. The applicant respectfully traverses.

Yamazaki shows in Figures 1A-1D and 2A-2D steps for forming memory cells with a source region in a substrate, a drain region in the substrate, an oxide film, a floating gate, and a control gate.

Halvis was discussed above.

The Office Action stated on pages 3-4 that it would have been obvious "to replace the polysilicon gate of Yamazaki with the floating gate of silicon carbide .... taught by Halvis .... because of the desirability to improve response, to improve quantum efficiency, and to improve performance and light sensitivity." The applicant respectfully traverses.

As stated above, there must be some suggestion or motivation to combine references to reject claims under 35 USC §103, and the suggestion or motivation must be found in the prior art.

Yamazaki shows a floating gate transistor, not a photodetector. Yamazaki discusses in the

background (text bridging columns 1 and 2) using ultraviolet (UV) irradiation to remove charge from a floating gate, but the gate of Halvis is fabricated from polysilicon with the addition of carbon to make the gate material more transparent to the **visible** portion of the energy spectrum, not the UV portion of the spectrum. There is no indication that the gate of Halvis would help in the erasing of the EPROM cell of Yamazaki.

In addition, Halvis says:

> "By adding carbon to the polysilicon material of a MOS photodector device, the amount of visible light absorbed by the gate material can be reduced, and the quantum efficiency of the detector can thereby be improved." Halvis, column 3, lines 30-35.

Halvis describes a gate that absorbs less visible light and is therefore more transparent to visible light. There is no indication in Yamazaki that a floating gate that is more transparent to visible light would improve the quantum efficiency of the floating gate transistor. The floating gate 107 of Yamazaki is covered by oxide 108 and is partially covered by the control gate 109. The oxide 108 and the partially covering control gate 109 would distort incoming visible light on the floating gate 107 of Yamazaki. There is also no indication in Yamazaki that the floating gate 107 is to be exposed to visible light for any reason. There is nothing in Yamazaki that would suggest to one skilled in the art to add carbon to the floating gate 107.

There is no suggestion for this combination of references.

The applicant respectfully submits that a *prima facie* case of obviousness of claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 has **not** been established in the Office Action, and that claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 are in condition for allowance.

Claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 were rejected under 35 USC § 103(a) as being unpatentable over Halvis taken with Tohyama (U.S. Patent No. 5,858,811) and Chamberlain. The applicant respectfully traverses.

Tohyama shows a charge coupled device (CCD). Halvis and Chamberlain were discussed above.

As stated above, there must be some suggestion or motivation to combine references to

reject claims under 35 USC §103, and the suggestion or motivation must be found in the prior art.

The office action stated that "[i]t would have been obvious ... to remove portions of the insulating layer and the layer of silicon carbide of Halvis in forming the gate as taught by Tohyama, wherein forming diffused regions functioned as source and drain regions ... is taught by Chamberlain. This is because of the desirability to control the desired thickness of the gate insulating layer... wherein source and drain regions are used for storing and transferring electrical charge." Office action, page 5.

Both of the structures shown by Halvis and Tohyama have gates or electrodes formed side-by-side over an insulating layer on a substrate. See the dielectric layer 32 of Halvis and the first and second gate oxide films 4 and 11 shown in Figs. 4A-4I of Tohyama. These insulating layers cover all of the substrate in both Halvis and Tohyama.

In contrast, the region D1 in Chamberlain must be exposed to light:

> "It is important to note that all parts of the photodetector structure are shielded from light except for region D1, the upper surface of which receives and is exposed to light." Chamberlain, column 3, lines 39-44.

One skilled in the art would **not** be motivated to put the gate structures of either Halvis or Tohyama over the region D1 of Chamberlain because the region D1 would then be covered by an insulating layer that would distort incoming light. There are no words in either Halvis, Tohyama, or Chamberlain that explain how this combination would work with an insulating layer over the region D1 of Chamberlain. There is no suggestion for this combination of references.

The applicant respectfully submits that a *prima facie* case of obviousness of claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 has **not** been established in the Office Action, and that claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 13 November 2002 By /Rea/

Robert E. Mates
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 13th day of November, 2002.

Name Amy Moriarty Signature /Amy Moriarty/